CLAIMS

What is claimed is:

1. A method of in-system programming of EEPROMs, the EEPROMs coupled to provide configuration code to programmable logic devices, each EEPROM being located on a particular circuit board of a plurality of circuit boards of a system and wherein not all EEPROMs are located on the same circuit board, comprising:

providing a plurality of board-specific serial busses, each board-specific serial bus coupling to EEPROMs of a particular circuit board;

coupling the plurality of board-specific serial busses to a common configuration point having selection apparatus;

coupling the common configuration point to configuration apparatus capable of interacting with at least one serial bus to program EEPROMs;

setting the selection apparatus to select a particular board-specific serial bus of the plurality of board-specific serial busses;

erasing at least one EEPROM coupled to the particular board-specific serial bus; and

writing programmable logic device configuration code through the selected board-specific serial bus to the at least one EEPROM.

2. The method of Claim 1, wherein the plurality of board-specific serial busses are of the JTAG type.

3. The method of Claim 2, wherein the programmable logic device configuration code comprises configuration code for at least one FPGA.

4. The method of Claim 3, further comprising the step of accessing the particular board-specific serial bus to verify compatibility of the code file with the selected circuit board.

5. The method of Claim 4, wherein at least one EEPROM device is collocated on the same die as at least one FPGA.

6. The method of Claim 4, further comprising the step of loading at least one of the programmable logic devices with configuration code from at least one of the EEPROMs.

7. Common connection point apparatus for in-system programming of EEPROMs, at least some of the EEPROMs coupled to provided code to programmable logic devices, each EEPROM located on a particular circuit board of a plurality of circuit boards of a system and where not all EEPROMs are located on the same circuit board, comprising:

interface apparatus for a plurality of serial busses, each serial bus intended for coupling to EEPROMs of a particular circuit board;

interface apparatus for connecting a configuration system;

selection apparatus for selecting a particular bus of the plurality of serial busses; and

coupling apparatus for coupling signals from the configuration system to the particular bus of the plurality of serial busses.

8. The connection point apparatus of Claim 7, wherein the serial busses are JTAG busses.

9. The connection point apparatus of Claim 8, wherein the selection apparatus comprises a switch settable by a technician.

10. The connection point apparatus of Claim 8, wherein the selection apparatus comprises a register addressable by the configuration apparatus.

11. A system comprising:

a plurality of interconnected circuit boards, at least two of the plurality of interconnected circuit boards embodying at least one FPGA coupled to a configuration EEPROM of the type capable of being programmed over a serial bus;

wherein at least one EEPROM of a circuit board of the plurality of circuit boards is coupled to a first serial bus, and at least one EEPROM of a circuit board of the plurality of circuit boards is coupled to a second serial bus;

common configuration point apparatus coupled to the first serial bus and to the second serial bus, the common configuration point apparatus further comprising:

selection apparatus for selecting a particular bus of the first and second serial busses; and

coupling apparatus for coupling configuration signals to the particular bus of the plurality of serial busses.

12. The system of Claim 10, wherein the first serial bus and the second serial bus are of the JTAG type.